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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/975,944	10/15/2001	Sudhakar Shenoy	CSCO-012/4912	9609

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EXAMINER	
WILSON, ROBERT W	

ART UNIT	PAPER NUMBER
2616	

DATE MAILED: 05/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/975,944	SHENOY ET AL.	
	Examiner	Art Unit	
	Robert W. Wilson	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4/18/06*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,10,18 and 23* is/are rejected.

7)☒ Claim(s) *2-9,11-17,19-21 and 24-27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 10, 18, & 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda (U.S. Patent No.: 6,711,167) in view of Bryenton (U.S. Patent No.: 6,826,184).

Referring to claim 1, Ikeda teaches: A first edge router (Figure 1) which is connected to an inherent second edge router (Figure 1) which converts IP packets or data grams into ATM cells or layer-2 packets per Fig 7 and per col. 7 line 55-col. 8 line 51.

The routers have a Lookup Table and VC Table per Fig 1 which contains a plurality of virtual circuits which are provisioned routes at the layer-2 level which are associated with IP header information or layer 3 routes per col. 9 lines 58-65 (Provisioning)

The first edge router (Figure 1) receives an IP packet or datagram as shown in Fig 7 (Receiving)

The first edge router defines or determines a subset of IP packets from IP layer-3 packets header information which determines the layer 3 route per col. 9 lines 58-65 (Determining)

The subset of layer-3 datagrams are encapsulated in a plurality of layer-2 packets as shown in Fig 7. Each of the layer-3 data gram associated with a given header information is assigned to the same virtual circuit per col. 9 lines 58-65 (Encapsulating)

Each of the ATM cells or layer-2 packets related to given IP header information are sent on the layer-2 network after they are encapsulated as shown in Fig 7.

Ikeda does not expressly call for: some of the subset of layer-3 datagrams being sent on a first one of said plurality of virtual circuits and all of the plurality of layer-2 packets corresponding to some other of said subset of layer-3 data grams being sent for transmission on another one of said plurality of virtual circuits.

Bryenton teaches: sending IP packets on different paths of virtual circuits based upon QoS or some of the subset of layer-3 datagrams being sent on a first one of said plurality of virtual circuits and all of the plurality of layer-2 packets corresponding to some other of said subset of layer-3 data grams being sent for transmission on another one of said plurality of virtual circuits. It would have been obvious to add the sending of subsets of packets on different virtual circuits of Bryenton to system where a subset of packets is sent down the same virtual circuit based upon header information of Ikeda in order to improve the quality of service by evaluating the QoS parameters in order to determine a layer-2 path.

Referring to claim 10, it is within the level of one skilled in the art at the time of the invention to implement the method of claim 1 in instructions. It would have been obvious to one of ordinary skill in the art at the time of the invention encode the software or instructions on a computer readable medium within the edge router in order for the instructions to be executable on a processor in the edge router.

Referring to claim 18, it is within the level of one skilled in the art at the time of the invention to implement the each of the method steps of claim 1 as logic or means because a method requires hardware or means in order to be implemented.

Referring to claim 23, Ikeda teaches: A first edge router (Figure 1) which is connected to an inherent second edge router (Figure 1) which converts IP packets or data grams into ATM cells or layer-2 packets per Fig 7 and per col. 7 line 55-col. 8 line 51.

The Lookup Table and VC table are memory which is used for storing data indicting that the plurality of virtual circuit are provided to the inherent second edge router (Figure 1) and the data (IP Packet per Fig 7) indicating the virtual circuits associated with a layer-3 route (Memory)

An inbound interface (First or Second Ethernet Interface per Fig 1) receiving said plurality of layer-3 data grams which are to be sent on a layer-3 route (Inbound Interface).

A virtual circuit determining block (8 per Fig 1) determining to sent a subset of layer-3 data grams on a virtual circuit (Virtual Circuit Determining Block)

An outbound interface (Outbound Interface to the ATM per Fig 1) sending each of the layer-3 data grams on one of the plurality of virtual circuits in the form of a plurality of layer-2 packets on the layer-2 network.

Ikeda does not expressly call for: some of the subset of layer-3 datagrams being sent on a first one of said plurality of virtual circuits and all of the plurality of layer-2 packets corresponding to some other of said subset of layer-3 data grams being sent for transmission on another one of said plurality of virtual circuits.

Bryenton teaches: sending IP packets on different paths of virtual circuits based upon QoS or some of the subset of layer-3 datagrams being sent on a first one of said plurality of virtual circuits and all of the plurality of layer-2 packets corresponding to some other of said subset of layer-3 data grams being sent for transmission on another one of said plurality of virtual circuits.

It would have been obvious to add the sending of subsets of packets on different virtual circuits of Bryenton to system where a subset of packets is sent down the same virtual circuit based upon header information of Ikeda in order to improve the quality of service by evaluating the QoS parameters in order to determine a layer-2 path.

Claim Objections

3. Claims 2-9, 11-17, 19-22, & 24-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Amendment

4. Applicant's arguments with respect to claims 1-30 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert W. Wilson whose telephone number is 571/272-3075. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Doris To can be reached on 571/272-7629. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Robert W Wilson
Examiner
Art Unit 2616

RWW
4/27/06

KEVIN C. HARPER
PATENT EXAMINER